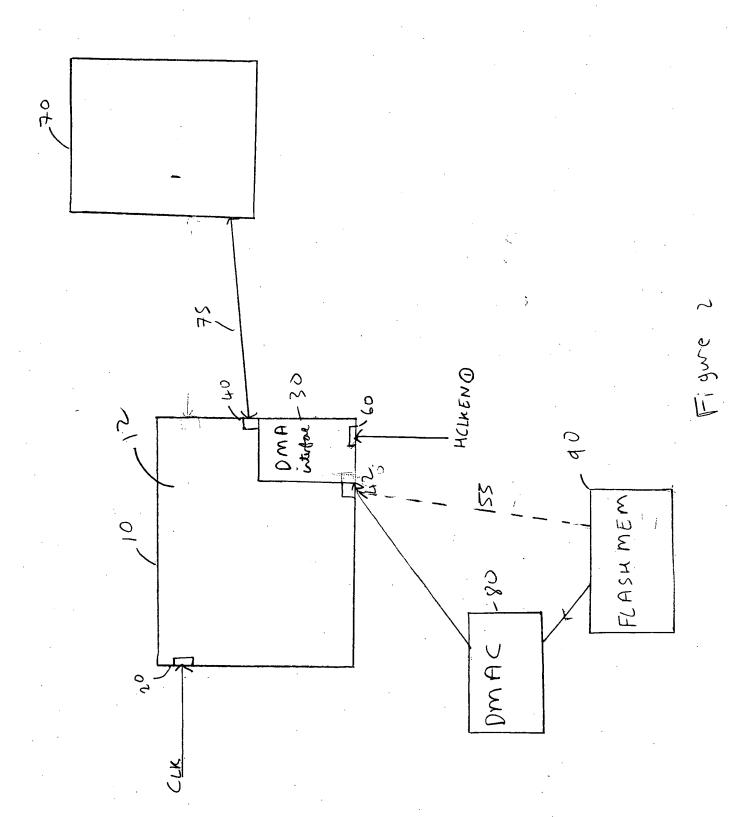


FI GLERE



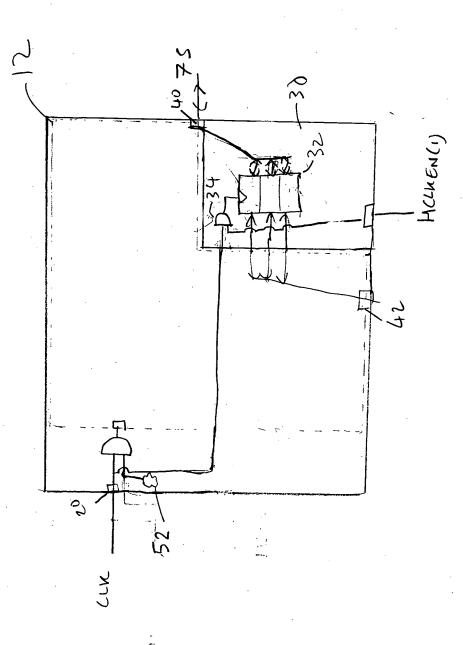


Figure S

4/7

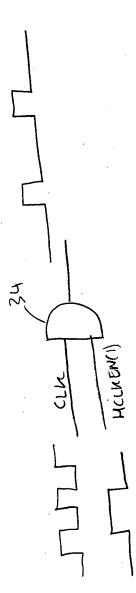
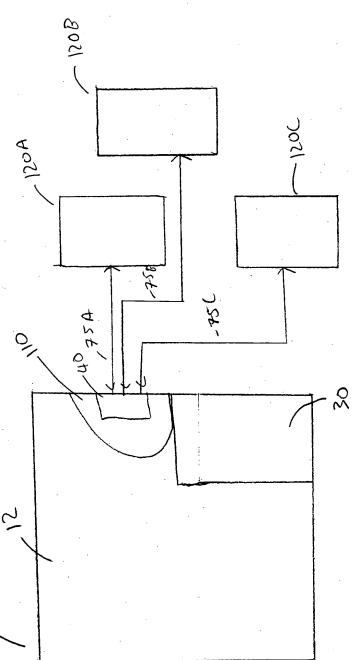


Figure 4







6/7

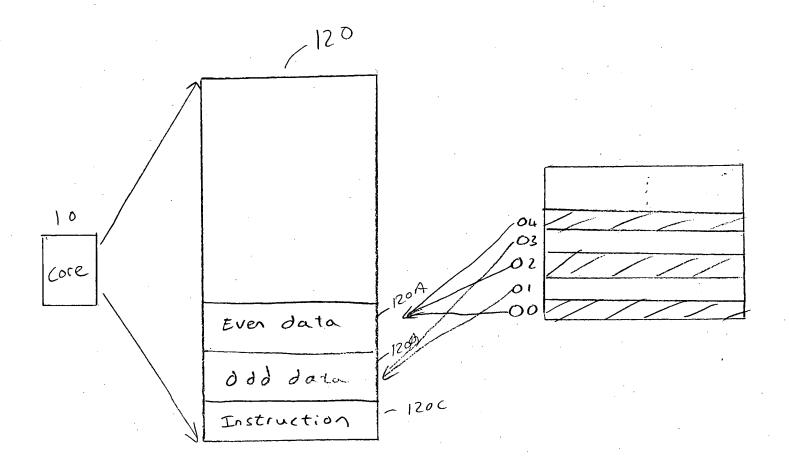


Figure 6

Receive Data access request 1 brom processing portion Receve data access request 2 from DM A interface address of data access request I and 2 in some memory portion? yes Poute data ouen regret 2 to menon yes route data acess request I tomomory

Figure 7

NO